One Week Faculty Development Program on "VLSI Design: bridging theory and practice"

in OFFLINE MODE from June 09 - 13, 2025

SCHEDULE

The title of the one week FDP : "VLSI Design: Bridging Theory and Practice " Mention the mode of The FDP: Offline							
Date/ Time	**9:30-11:00**	**11:00-11:30**	**11:30-1:00**		**14:00 - 15:30**	**15:30 – 16:00**	**16:00 – 17:30**
Day 1	Registration/Inauguration Expert Lecture by Dr. Manoj Saxena Professor, Department of Electronics Deen Dayal Upadhyaya College, University of Delhi, Dwarka Sector-3, New Delhi-110078, India	**HIGH TEA**	Expert Lecture by Dr. Balwinder Singh, Joint Director & Head, Academic and Consultancy Services Division, Centre for Development of Advanced Computing (C-DAC),Ministry of Electronics and IT , A-34 Phase VIII, Industrial Area, Mohali(PB)	**Lunch Break (13:00-14:00)**	Introduction to VLSI design flow Basics of Digital Logic Design and Introduction to HDL tools By Dr. Balwinder Singh	**HIGH TEA**	Introduction to HDL & different levels of abstraction, operator By. Ms. Soniya
Day 2	Expert Lecture by Prof. Rajendra Singh, Professor at the Department of Physics, IIT Delhi; Principal Investigator of the Advanced Semiconductor Materials and Devices Group; Joint Faculty at the Department of Electrical Engineering, IIT Delhi		Expert Lecture by Dr. Balwinder Singh, Joint Directro& Head, Academic and Consultancy Services Division, Centre for Development of Advanced Computing (C-DAC),Ministry of Electronics and IT , A-34 Phase VIII,Industrial Area ,Mohali(PB)		Practical session On Combinational logic design fundamentals (HA, FA, MUX, DMUX) By Dr. Balwinder Singh and Ms. Soniya	**HIGH TEA**	Session on "Insights of IEEE" by Prof. Shruti Jain, Joint Secretary, IEEE Delhi Section, Member MDC, Delhi Section Session on "NEP implementation in Higher Education Institutes" by NEP coordinator Prof. Rakesh Kumar Bajaj, HoD, Mathematics Department.

Day 3	Introduction to Sequential Circuit Design By Dr. Pardeep Garg, JUIT		Sequential Circuit Design Exercise (Latch, Flip-Flops, Register, Counters) By Dr. Shruti Jain, JUIT		Practical Session on Sequential Circuit Design Exercise By Dr. Pardeep Garg, JUIT	**HIGH TEA**	Practical Session on Sequential Circuit Design Exercise Minor project allotment in groups By Dr. Vikas Baghel, JUIT
Day 4	Introduction to FPGA Architecture and Development Flow By Dr. Shruti Jain, JUIT		FPGA Implementation, Debugging, Mr. Prathamesh Centre for Development of Advanced Computing (C-DAC),Ministry of Electronics and IT , A-34 Phase VIII,Industrial Area ,Mohali(PB)		FPGA Implementation, Debugging, Mr. Prathamesh	**HIGH TEA**	Conduct of Minor Projects Dr. Nishant Jain and Dr. Vikas Baghel
Day 5	Expert Lecture by Prof. Sudeb Dasgupta, Professor, in Microelectronics and VLSI Group in the Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee.		Expert Lecture by Prof. H.S. Jatana Working in CMOS process development & Integration, and VLSI Design at DSM. Expertise - Space/Mil grade Product development, now at PGIMER & Adjunct Faculty at Reputed Institutions		Evaluation / Discussion/ Test Dr. Nishant Jain and Dr. Vikas Baghel	**HIGH TEA**	Valedictory