REPORT
of
Faculty Development Program (FDP)
on
VLSI DESIGN: BRIDGING THEORY AND PRACTICE
Date: June 09 – 13, 2025

The Department of Electronics & Communication Engineering, Jaypee University of Information Technology (JUIT), in collaboration with Electronics & ICT Academy, Centre for Development of Advanced Computing (CDAC), Mohali, IEEE R10 EAC, IEEE India Council, IEEE Delhi Section, IEEE MDC, SAC, and WIE AG Delhi Section, successfully organized a one-week Faculty Development Program (FDP) on "**VLSI Design: Bridging Theory and Practice**" from June 9 to June 13, 2025.

The FDP was formally inaugurated with an inspiring address by the Chief Guest, Mr. V.K. Sharma, Scientist-G and Director at CDAC Mohali. He underscored the growing relevance of semiconductor design in India's national development, emphasizing the role of academic institutions in fostering technological leadership and research capabilities. His insights effectively set the tone for the sessions that followed.

The FDP aimed to bridge the gap between academic teaching and industry demands by covering advanced topics such as digital and analog VLSI design, FPGA implementation, and design automation, along with practical sessions using industry-standard tools like Cadence and Xilinx Vivado.

The program brought together eminent experts from academia, industry, and research organizations, as reflected in the distinguished speaker lineup:

1. Dr. Balwinder Singh, Scientist-E, CI, E&ICT Academy, CDAC Mohali, served as both Guest of Eminence and Resource Person.
2. Prof. Manoj Saxena, Department of Electronics, University of Delhi, graced the event as Guest of Honor and Resource Person.
3. Prof. Rajendra Singh, Department of Physics, IIT Delhi contributed as resource persons.
4. Prof. Sudeb Dasgupta, Department of ECE, IIT Roorkee contributed as resource persons.
5. Mr. Harpreet S. Jatana, Former Group Head, SCL Mohali and ISRO, brought industry depth as a senior resource person.

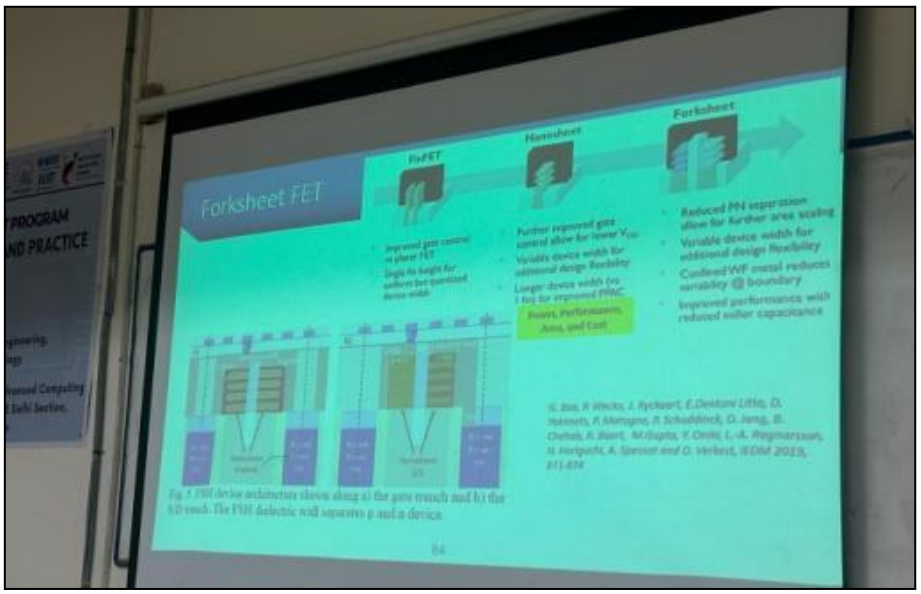
The event hosted 42 participants from 28 institutions across 13 states, including faculty, research scholars, and JRFs from renowned institutes, fostering a vibrant exchange of ideas. The FDP consisted of expert lectures along with hands-on projects. The FDP was coordinated by Prof. Shruti Jain, Dr. Vikas Baghel, Dr. Nishant Jain, and Dr. Pardeep Garg.


Department of Electronics & Communication Engineering,
Jaypee University of Information Technology
in collaboration with
Electronics & ICT Academy, Centre for Development of Advanced Computing
(C-DAC), Mohali, IEEE R10 EAC, IEEE India Council, IEEE Delhi Section,
IEEE MDC, SAC and WIE AG Delhi Section
Organizing
One Week FACULTY DEVELOPMENT PROGRAM
VLSI DESIGN: BRIDGING THEORY AND PRACTICE
JUNE 09 - 13, 2025
Chief Guest
Mr. V.K. Sharma
Scientist-G, Director
CDAC Mohali
Guest of Eminence
& Resource Person
Dr. Balwinder Singh
Scientist-E, CI, E&ICT Academy
CDAC Mohali
Guest of Honor
& Resource Person
Prof. Manoj Saxena
Department of Electronics
University of Delhi
Resource Person
Prof. Rajendra Singh
Department of Physics
IIT Delhi
Resource Person
Prof. Sudeb Dasgupta
Department of ECE
IIT Roorkee
Resource Person
Mr. Harpreet S. Jatana
Former Group Head
SCL Mohali and ISRO

Session Highlights

Day 1, Session 1

Day 1, Session 1 commenced with an expert lecture by Prof. Manoj Saxena, Department of Electronics, University of Delhi. His session, titled *"100 Years of FET: Development and Innovations"*, traced the historical journey of field-effect transistors and their role in shaping modern electronics. He provided a wide-ranging discussion—from fundamental theories to IC design challenges and pedagogical practices—enriching the knowledge base of all participants.

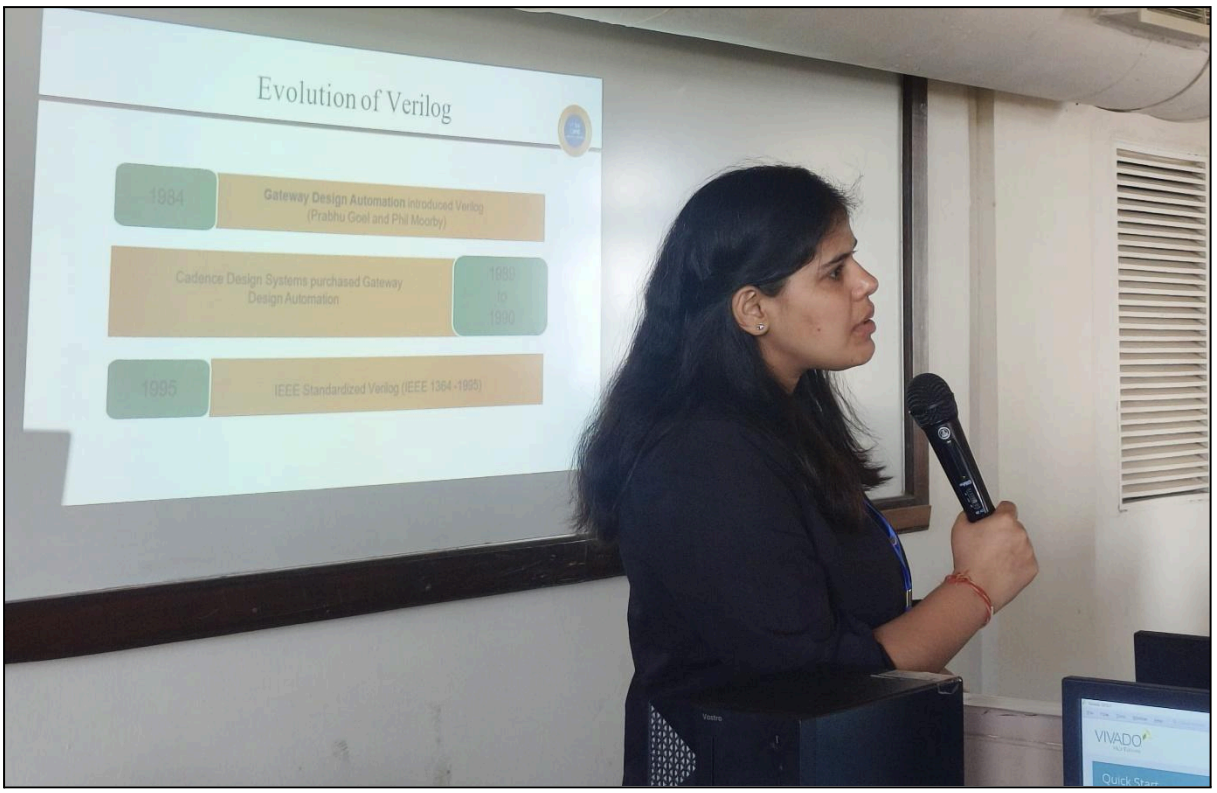


Day 1, Session 2

Day 1, Session 2 featured Dr. Balwinder Singh, Scientist-E at CDAC Mohali. His lecture on *"Chip Design: From Sand to System on Design"* provided a comprehensive view of the semiconductor development lifecycle. He delivered an insightful session on the complete chip design process—from raw silicon to system-level integration. He explained key semiconductor fabrication steps like oxidation, photolithography, etching, doping, and metallization. The VLSI design cycle was covered in detail, from specification and HDL-based design to fabrication and testing. Dr. Singh also introduced Programmable Logic Devices (FPGAs, CPLDs) and their role in rapid prototyping. Foundational concepts of logic design, including Boolean algebra and gate-level circuits, were revisited. The session concluded with a deep dive into N-MOS fabrication and the concept of System on Design (SoD), emphasizing compact, multi-functional chip integration used in modern devices.

Day 1, Session 3

Day 1 – Session 3 Ms. Soniya Badgujjar delivered an expert lecture on *"Basics of Digital Logic Design and Introduction to HDL,"* focusing on core digital design concepts and practical Verilog implementation. She covered logic gates, Boolean algebra, and combinational circuits, followed by an introduction to Verilog syntax, identifiers, keywords, and hierarchical design. The session included hands-on practice with designing and simulating basic circuits like adders and multiplexers. This blend of theory and application provided participants with a solid foundation in digital logic and HDL programming.



Day 2, Session 1

Day 2, Session 1 featured Prof. Rajendra Singh, Department of Physics and Electrical Engineering, IIT Delhi, titled *"Semiconductor Manufacturing in India: Role of Academia."* Prof. Singh provided a comprehensive overview of India's growing semiconductor ecosystem, emphasizing the importance of academic involvement in research, innovation, and industry collaboration. He discussed the India Semiconductor Mission (ISM), the fabrication of single-crystalline silicon wafers, and key initiatives like the Nanoscale Research Facility (NRF) and Indian Nanoelectronics Users Program (INUP), inspiring participants to actively contribute to India's semiconductor future.

Day 2 – Session 2

Day 2 – Session 2 conducted by Dr. Balwinder Singh, Scientist-E, CI, E&ICT Academy, CDAC Mohali, titled *"Chip Design: From Sand to System on Design."* As part of the Faculty Development Programme on VLSI Design, Dr. Singh provided a detailed walkthrough of the entire semiconductor development process—from silicon extraction to the final integrated circuit. He covered key topics such as logic design fundamentals, the conversion of sand into high-purity silicon wafers, and the fabrication steps involved in N-MOS technology. The session also introduced participants to clean room requirements and highlighted the full chip development cycle, emphasizing the significance of academic involvement in advancing India's chip design capabilities.

Day 2 – Session 3

Day 2 – Session 3 was conducted by Ms. Soniya Badgujjar, Project Engineer at C-DAC Mohali, titled *"Basics of Digital Logic Design and Introduction to HDL."* She introduced participants to key HDL concepts, including identifiers, keywords, data types, number representation, and operators. The session also covered designing combinational circuits using various abstraction levels—behavioral, RTL, and structural—with practical examples in Verilog and VHDL. The lecture effectively bridged theoretical logic design with hands-on HDL implementation, providing a solid foundation for beginners in digital design and VLSI.

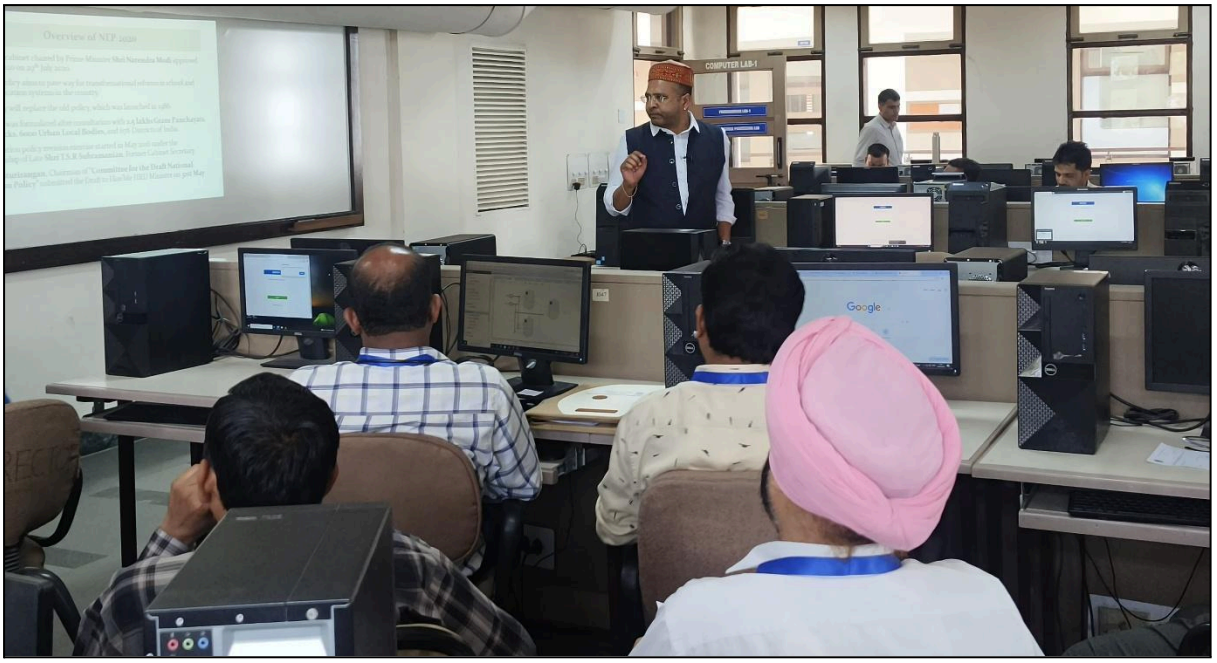
Day 2 – Session 4

Day 2 – Session 4 featured by Prof. Rakesh Kumar Bajaj from JUIT, Waknaghat, on *"National Education Policy 2020"* and Prof. Shruti Jain, Associate Dean (Innovation) at JUIT, who spoke on "Explore the IEEE Member Experience".

Prof. Rakesh Kumar Bajaj provided a comprehensive overview of NEP 2020, highlighting its emphasis on multidisciplinary education, academic flexibility, research funding, and

institutional autonomy. Key reforms such as MERUs, ABC, and the Multiple Entry-Exit system were discussed alongside core themes like equity, technology integration, and teacher empowerment. Prof. Bajaj also emphasized the Malaviya Mission for faculty capacity building, making the session highly relevant for aligning academic practices with national education reforms.

Prof. Shruti Jain spoke on *"Explore the IEEE Member Experience."* She presented an overview of IEEE's global impact, professional benefits, and opportunities for academic engagement. Her talk encouraged faculty and students to actively participate in IEEE activities, including technical societies, volunteering roles, and coding competitions that enhance career and research prospects.

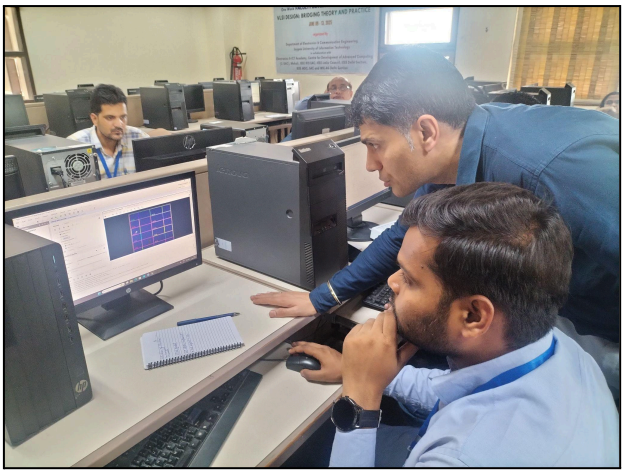


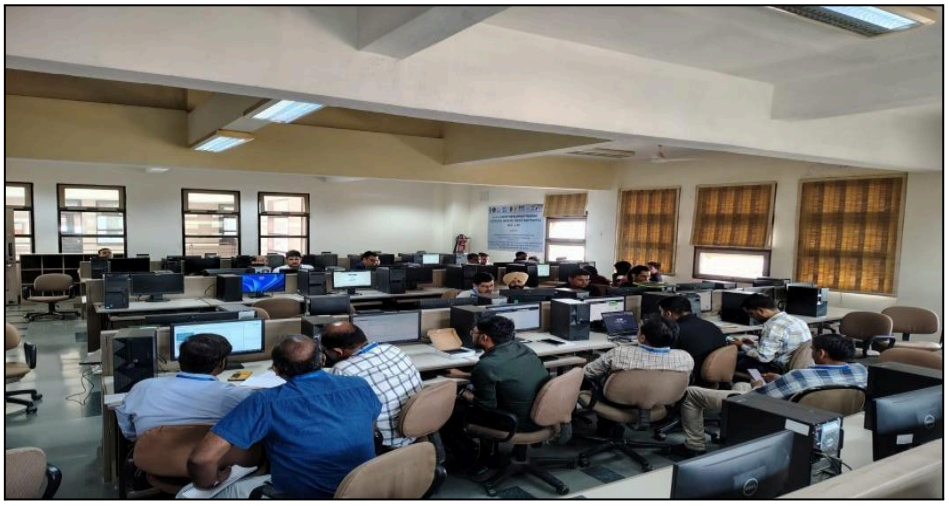
Day 3 – Session 1

Day 3, Session 1 consisted of a collaborative expert lecture by Dr. Shruti Jain and Dr. Pardeep Garg from JUIT, titled *"Introduction to Sequential Circuit Design."* The session introduced the concepts of flip-flops, finite state machines, timing analysis, and register design. Participants engaged in practical design exercises using simulation tools and were grouped into teams to work on minor projects. The guided, hands-on format provided deep practical learning.

Day 3 – Session 2

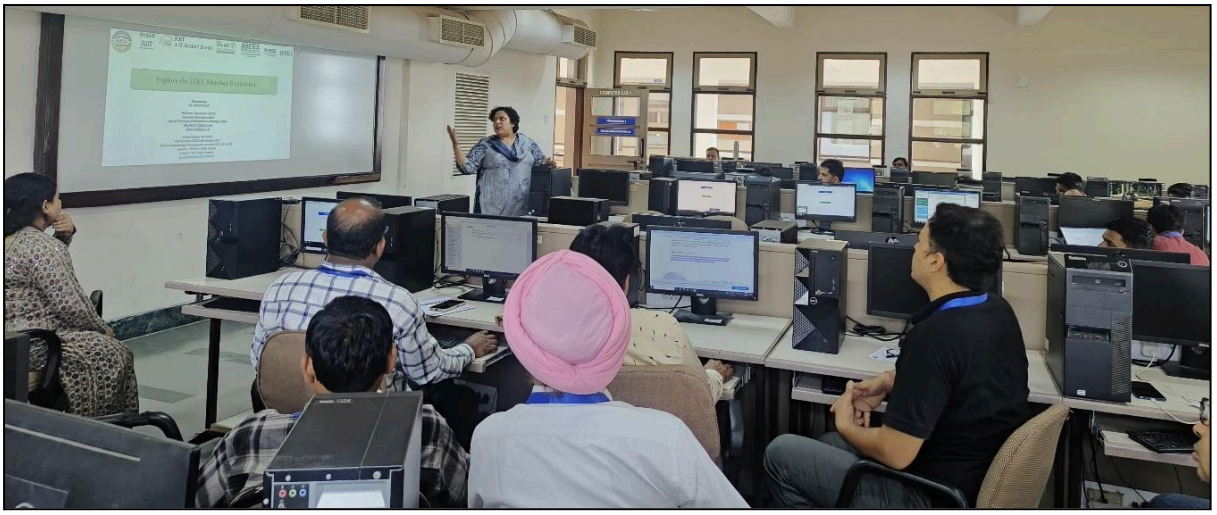
Day 3, Session 2 consisted of a collaborative expert lecture by Dr. Vikas Baghel and Dr.Pardeep Garg from JUIT, titled *"Practical Sequential Circuit Design Exercises"*. Participants engaged in practical design exercises using simulation tools and were grouped into teams to work on minor projects. The guided, hands-on format provided deep practical learning.





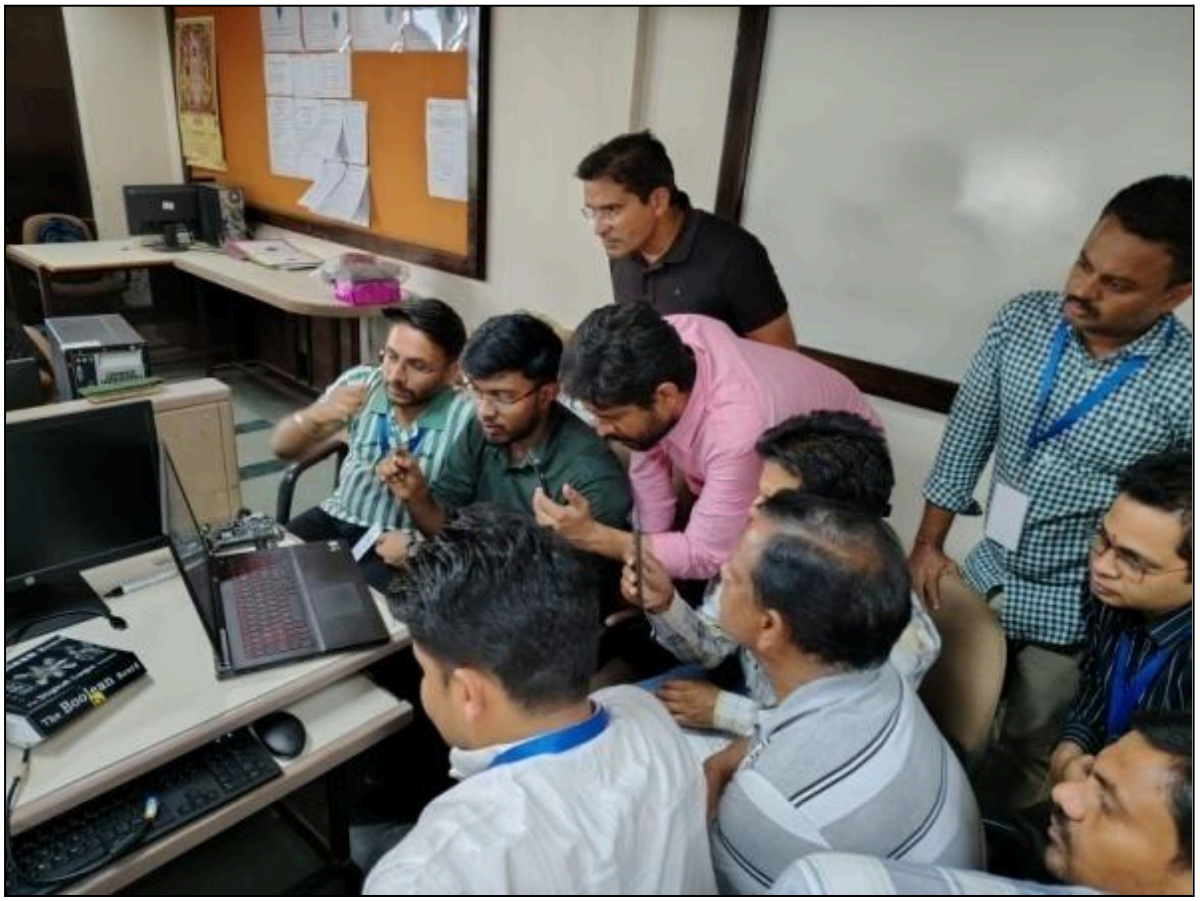
Day 4, Session 1

Day 4 – Session 1 was conducted by Prof. Shruti Jain, Associate Dean (Innovation) at JUIT, on "Introduction to FPGA Architecture and Development Flow". The session by Prof. Shruti Jain provided a comprehensive overview of FPGA fundamentals, including their programmable logic blocks, interconnects, and configurable I/O. The lecture detailed the key stages of FPGA development, from design entry and synthesis to implementation and programming, emphasizing tools like HDL (Hardware Description Language) and FPGA-specific software. Prof. Jain highlighted best practices for efficient design, optimization techniques, and common challenges faced during FPGA development, offering students practical insights into the architecture and development flow essential for designing complex digital systems.



Day 4, Session 2

Day 4, Session 2 was conducted by Mr. Prathamesh, Project Engineer at CDAC Mohali. He delivered two consecutive sessions: *"Introduction to FPGA Architecture and Development Flow"* and *"FPGA Implementation, Debugging, and Minor Projects."* He explained core FPGA components such as CLBs and LUTs, and demonstrated implementation using tools like Xilinx Vivado. He also showcased debugging tools like ILAs and discussed real-time project ideas. The sessions promoted interactive learning and empowered participants to start FPGA-based projects.



Day 5, Session 1

Day 5, Session 1 featured a highly specialized lecture by Prof. Sudeb Dasgupta from IIT Roorkee on *"Cryo-CMOS: Bridging Classical Readout and Quantum Hardware at 4.2K Temperature."* He discussed the design of CMOS circuits that operate under cryogenic

conditions—critical for quantum computing applications. His discussion spanned cryo-compatible device modeling, challenges at low temperatures, and potential future directions in hybrid classical-quantum system integration.

Day 5, Session 2

Day 5, Session 2 concluded the technical sessions of the FDP with an expert lecture by Prof. H.S. Jatana, an authority in deep submicron (DSM) technologies and space-grade VLSI systems. His lecture, titled *"Challenges in Development of Space Grade VLSI Products in DSM Regime"*, addressed the design, fabrication, and reliability demands of electronics used in aerospace and defense. He explained techniques for radiation hardening, reliability testing, and process customization. Drawing from industry experience, he presented practical challenges and case studies that added immense value for all participants.

Valedictory session

Following Prof. Jatana's engaging session, the valedictory session was held to officially close the Faculty Development Program. Participants reflected on the technical richness and practical orientation of the sessions, appreciating the diversity of topics and quality of resource persons. Certificates were distributed, and the organizing team expressed gratitude to all collaborators, speakers, and attendees for making the program a resounding success.

List of Participants

S.N	Title	Name	Gender	Designation	Department	Type of Institute	Affiliation
1	Mr.	Shashwat Anand Pandey	Male	Project Intern AMU, Aligarh	Electronics Engineering	Engineering Institute/University	Aligarh Muslim University
2	Mr.	Uttam Kumar Gupta	Male	Faculty	Electrical Engineering	Engineering Institute/University	Anand International College of Engineering, Jaipur
3	Mr.	Ankit Kumar Sharma	Male	Faculty	Electrical engineering	Engineering Institute/University	Anand International College of Engineering, Jaipur
4	Dr.	M.SARAVANAN	Male	Faculty	Electronics & Communication Engineering	Engineering Institute/University	Annamalai University
5	Dr.	Arvinder Kaur	Female	Faculty	Information Technology	College	Chandigarh Engineering College-CGC, Landran, Mohali
6	Dr.	Swapnali Ashish Makdey	Female	Faculty	Electronics and Computer Science	Engineering Institute/University	Fr.conceicao Rodrigues college of engineering
7	Mr.	Rishabh Yadav	Male	Faculty	Electronics & Communication Engineering	Engineering Institute/University	GL Bajaj Institute of Technology and Management, Greater Noida
8	Mr.	SAT PAL	Male	Faculty	Technical Education Vocational Industrial Training Sundernagr Himachal	Polytechnic / ITI / STEM	Govt Industrial Training Institute (ITI) for Persons with Disabilities

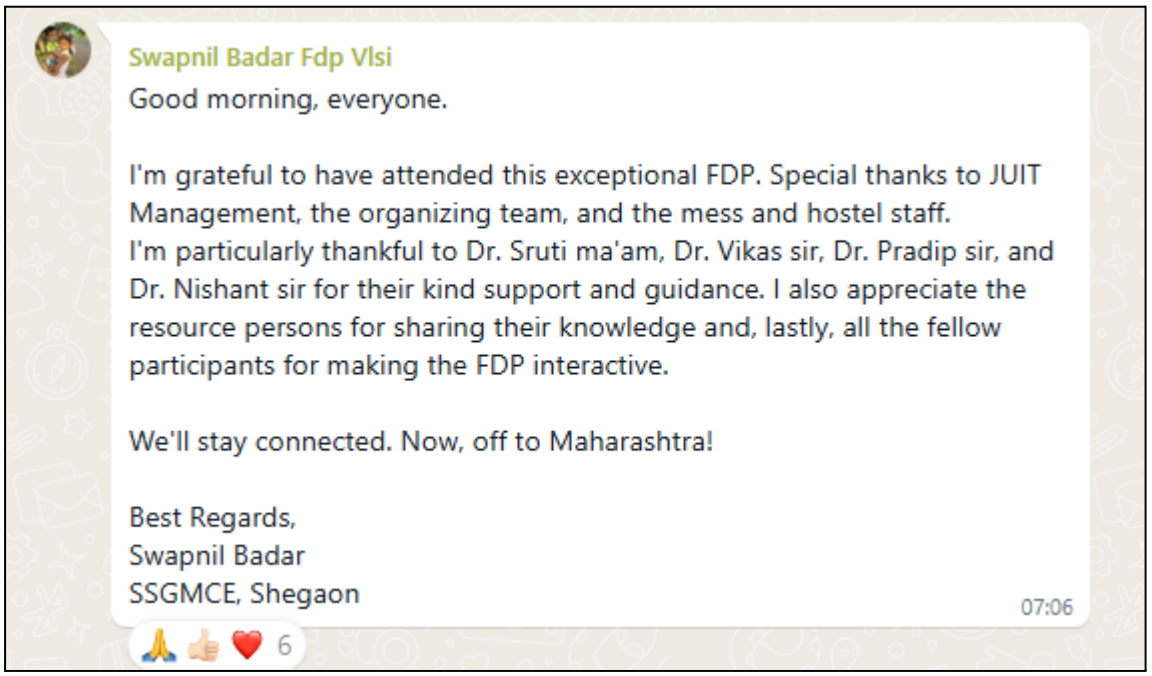
					Pradesh		Sundernagar
9	Mr.	Mohit Kumar Banger	Male	Senior Lecturer	Electronics & Communication Engineering	Polytechnic	Government Polytechnic, Sirsa
10	Mr.	Kavam Dhillon	Male	Junior Research Fellow	Department of Physics	Engineering Institute/University	Indian institute of Technology Delhi
11	Dr.	H. P. Agrawal	Male	Faculty	Electrical and Electronics Engineering	Engineering Institute/University	JK Lakshmipat University, Jaipur
12	Prof.	Gaurav Mani Khanal	Male	Faculty	Electrical and Electronics Engineering	Engineering Institute/University	JK Lakshmipat University, Jaipur
13	Mr.	Divanshu Jain	Male	Faculty	Electrical and Electronics Engineering	Engineering Institute/University	JK Lakshmipat University, Jaipur
14	Dr.	Ankush Manocha	Male	Faculty	School of computer applications	Engineering Institute/University	Lovely Professional University
15	Dr.	Devender Kumar	Male	Faculty	School of computer applications	Engineering Institute/University	Lovely Professional University,Phagwara
16	Mr.	Gurmeet Singh	Male	Faculty	Information Technology	College	M.L.N College, Yamuna Nagar
17	Dr.	Amit Saxena	Male	Faculty	Electronics & Communication Engineering	Engineering Institute/University	Maharaja Agrasen Institute of Technology
18	Mr.	Ram Kumar	Male	Lab Staff	Electronics & Communication Engineering	Engineering Institute/University	Maharaja Agrasen Institute of Technology
19	Mr.	Manoj Kumar Tomar	Male	Research Scholar	Electronics & Communication Engineering	Engineering Institute/University	Maharaja Agrasen Institute of Technology

20	Dr.	UMESH CHANDRA SINGH	Male	Faculty	Electronics & Communication Engineering	Engineering Institute/University	Maharaja Agrasen Institute Of Technology
21	Dr.	Jagpreet	Male	Faculty	STME	Engineering Institute/University	NMIMS, Chandigarh campus
22	Dr.	Rajesh Singh	Male	Faculty	Electronics	College	RKSD College, Kaithal
23	Dr.	Nisha Chugh	Female	Faculty	Electronics Engineering (VLSI Design & Technology)	Engineering Institute/University	School of Engineering and Technology, Vivekanand Institute of Professional Studies-Technical Campus, Pitampura, New Delhi-110034
24	Dr.	Yugal Kumar	Male	Faculty	Department of Computer Engineering	Engineering Institute/University	School of Technology Management and Engineering NMIMS Deemed to be University Chandigarh Campus
25	Prof.	Tejrao Panjabrao Marode	Male	Faculty	Electronics and Telecommunication Engineering	Engineering Institute/University	Shri Sant Gajanan Maharaj College of engineering Shegaon
26	Dr.	Swapnil Panjabrao Badar	Male	Faculty	Electronics and Telecommunication Engineering	Engineering Institute/University	Shri Sant Gajanan Maharaj College of Engineering,

							Shegaon
27	Dr.	Kamlesh Tulshiram Kahar	Male	Faculty	Electronics and Telecommunication Engineering	Engineering Institute/University	Shri Sant Gajanan Maharaj College of Engineering, Shegaon
28	Mr.	Parbhat Gupta	Male	Faculty	Computer Science and Engineering	Engineering Institute/University	SRM Institute of Science and Technology, Delhi-NCR Campus
29	Dr.	Dinesh Kumar	Male	Faculty	Computer Science and Engineering	Engineering Institute/University	SRM Institute of Science and Technology, Delhi-NCR Campus
30	Mr.	Amar Chandra	Male	Faculty	Computer Science and Engineering	Engineering Institute/University	SRM Institute of Science and Technology, Delhi-NCR Campus
31	Mrs.	Jyotsana Bajaj	Female		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
32	Dr,	Ajay Kumar Singh	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
33	Mr.	Dhirendra Singh	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
34	Mr.	Shambhoo	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
35	Mr.	Harish	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology

36	Ms.	Shilpa Kaushal	Female		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
37	Ms.	Ritika	Female		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
38	Mr.	Anmol Shalom Rathore	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
39	Dr.	Shruti Jain	Female		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
40	Dr.	Vikas Baghel	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
41	Dr.	Nishant Jain	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology
42	Dr.	Pardeep Garg	Male		Electronics & Communication Engineering	Engineering University	Jaypee University of Information Technology

Feedbacks



Swapnil Badar Fdp Vlsi

Good morning, everyone.

I'm grateful to have attended this exceptional FDP. Special thanks to JUIT Management, the organizing team, and the mess and hostel staff.
I'm particularly thankful to Dr. Sruti ma'am, Dr. Vikas sir, Dr. Pradip sir, and Dr. Nishant sir for their kind support and guidance. I also appreciate the resource persons for sharing their knowledge and, lastly, all the fellow participants for making the FDP interactive.

We'll stay connected. Now, off to Maharashtra!

Best Regards,
Swapnil Badar
SSGMCE, Shegaon

07:06

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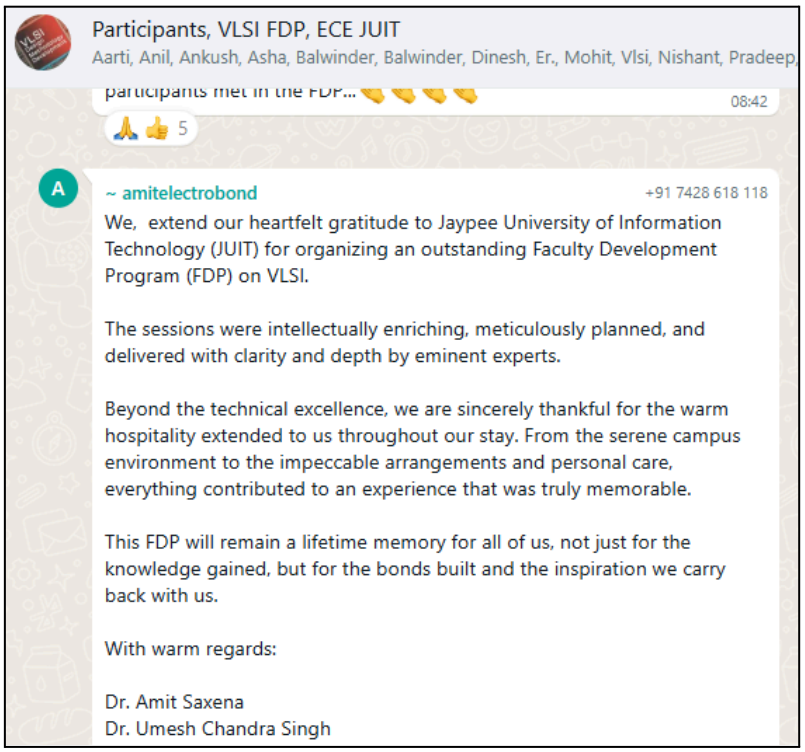


Participants, VLSI FDP, ECE JUIT

Aarti, Anil, Ankush, Asha, Balwinder, Balwinder, Dinesh, Er., Mohit, Vlsi, Nishant, Pradeep,

participants met in the FDP... 👏 👏 👏 👏

08:42

🙏 👍 5

A ~ amitelectrobond +91 7428 618 118

We, extend our heartfelt gratitude to Jaypee University of Information Technology (JUIT) for organizing an outstanding Faculty Development Program (FDP) on VLSI.

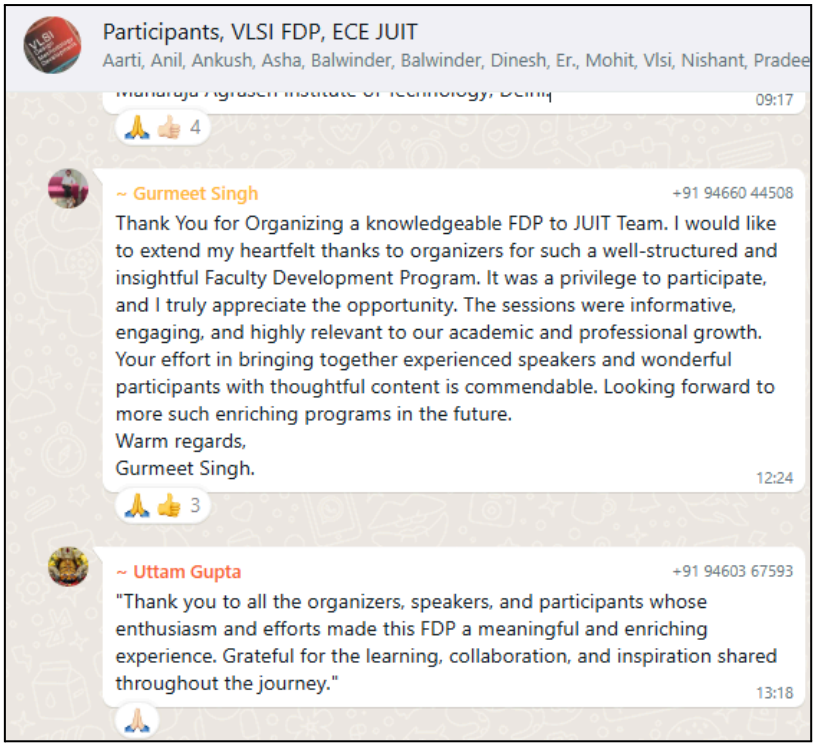
The sessions were intellectually enriching, meticulously planned, and delivered with clarity and depth by eminent experts.

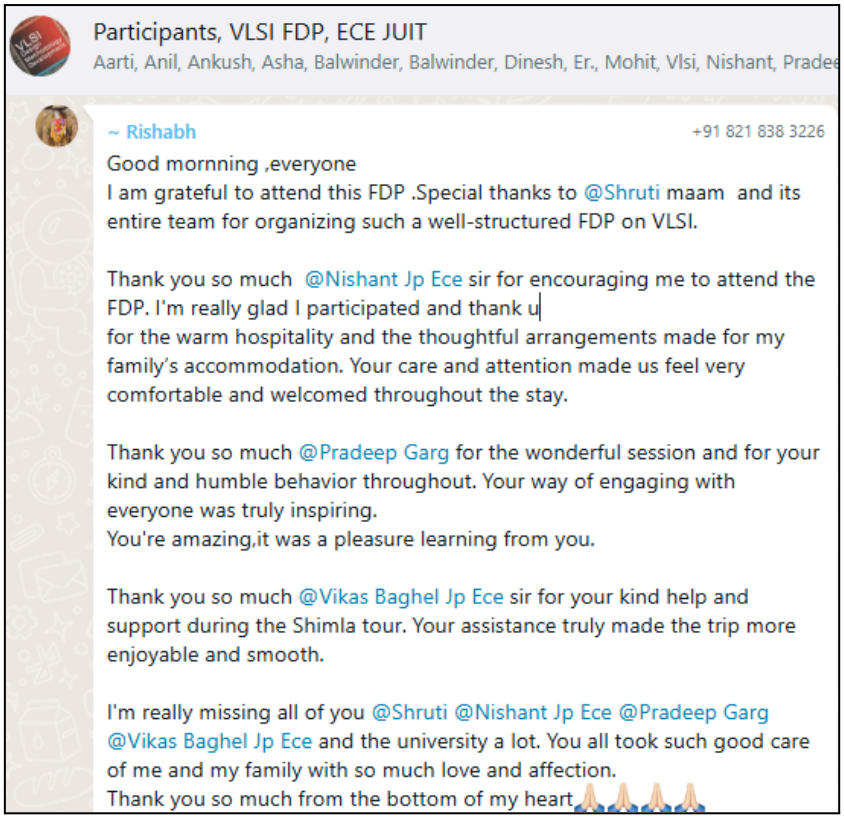
Beyond the technical excellence, we are sincerely thankful for the warm hospitality extended to us throughout our stay. From the serene campus environment to the impeccable arrangements and personal care, everything contributed to an experience that was truly memorable.

This FDP will remain a lifetime memory for all of us, not just for the knowledge gained, but for the bonds built and the inspiration we carry back with us.

With warm regards:

Dr. Amit Saxena
Dr. Umesh Chandra Singh


Participants, VLSI FDP, ECE JUIT
Aarti, Anil, Ankush, Asha, Balwinder, Balwinder, Dinesh, Er., Mohit, Vlsi, Nishant, Pradee
09:17
4
~ Gurmeet Singh
+91 94660 44508
Thank You for Organizing a knowledgeable FDP to JUIT Team. I would like to extend my heartfelt thanks to organizers for such a well-structured and insightful Faculty Development Program. It was a privilege to participate, and I truly appreciate the opportunity. The sessions were informative, engaging, and highly relevant to our academic and professional growth. Your effort in bringing together experienced speakers and wonderful participants with thoughtful content is commendable. Looking forward to more such enriching programs in the future.
Warm regards,
Gurmeet Singh.
12:24
3
~ Uttam Gupta
+91 94603 67593
"Thank you to all the organizers, speakers, and participants whose enthusiasm and efforts made this FDP a meaningful and enriching experience. Grateful for the learning, collaboration, and inspiration shared throughout the journey."
13:18


Participants, VLSI FDP, ECE JUIT
Aarti, Anil, Ankush, Asha, Balwinder, Balwinder, Dinesh, Er., Mohit, Vlsi, Nishant, Pradee
~ Rishabh
+91 821 838 3226
Good mornning ,everyone
I am grateful to attend this FDP .Special thanks to @Shruti maam and its entire team for organizing such a well-structured FDP on VLSI.
Thank you so much @Nishant Jp Ece sir for encouraging me to attend the FDP. I'm really glad I participated and thank u
for the warm hospitality and the thoughtful arrangements made for my family's accommodation. Your care and attention made us feel very comfortable and welcomed throughout the stay.
Thank you so much @Pradeep Garg for the wonderful session and for your kind and humble behavior throughout. Your way of engaging with everyone was truly inspiring.
You're amazing,it was a pleasure learning from you.
Thank you so much @Vikas Baghel Jp Ece sir for your kind help and support during the Shimla tour. Your assistance truly made the trip more enjoyable and smooth.
I'm really missing all of you @Shruti @Nishant Jp Ece @Pradeep Garg @Vikas Baghel Jp Ece and the university a lot. You all took such good care of me and my family with so much love and affection.
Thank you so much from the bottom of my heart

Social Media Coverage:

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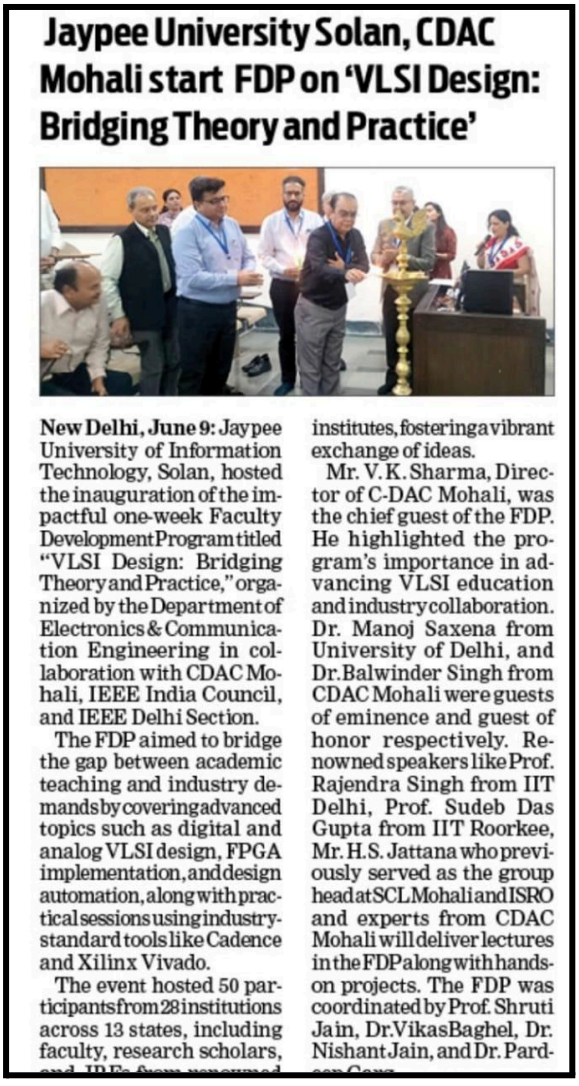
Newspaper Coverage



Jaypee University Solan, CDAC Mohali start FDP on 'VLSI Design: Bridging Theory and Practice'

New Delhi, June 9: Jaypee University of Information Technology, Solan, hosted the inauguration of the impactful one-week Faculty Development Program titled "VLSI Design: Bridging Theory and Practice," organized by the Department of Electronics & Communication Engineering in collaboration with CDAC Mohali, IEEE India Council, and IEEE Delhi Section.

The FDP aimed to bridge the gap between academic teaching and industry demands by covering advanced topics such as digital and analog VLSI design, FPGA implementation, and design automation, along with practical sessions using industry-standard tools like Cadence and Xilinx Vivado.

The event hosted 50 participants from 28 institutes across 13 states, including faculty, research scholars, and JRFs from renowned institutes, fostering a vibrant exchange of ideas.

Mr. V.K. Sharma, Director of C-DAC Mohali, was the chief guest of the FDP. He highlighted the program's importance in advancing VLSI education and industry collaboration. Dr. Manoj Saxena from University of Delhi, and Dr. Balwinder Singh from CDAC Mohali were guests of eminence and guest of honor respectively. Renowned speakers like Prof. Rajendra Singh from IIT Delhi, Prof. Sudeb Das Gupta from IIT Roorkee, Mr. H.S. Jattana who previously served as the group head at SCL Mohali and ISRO and experts from CDAC Mohali will deliver lectures in the FDP along with hands-on projects. The FDP was coordinated by Prof. Shruti Jain, Dr. Vikas Baghel, Dr. Nishant Jain, and Dr. Pardeep Garg

जेपी यूनिवर्सिटी ने की 'वीएलएसआई डिजाइन ब्रिजिंग थ्योरी एंड प्रैक्टिस' कार्यक्रम के उद्घाटन की मेजबानी

हिमाचल दस्तक ॥ सोलन

जेपी सूचना प्रौद्योगिकी विश्वविद्यालय, सोलन ने इलेक्ट्रॉनिक्स और संचार इंजीनियरिंग विभाग की ओर से सीडैक मोहाली, आईईईई इंडिया काउंसिल और आईईईई दिल्ली सेक्शन के सहयोग से आयोजित 'वीएलएसआई डिजाइन ब्रिजिंग थ्योरी एंड प्रैक्टिस' नामक प्रभावशाली एक सप्ताह के संकाय विकास कार्यक्रम के उद्घाटन की मेजबानी की। एफडीपी का उद्देश्य डिजिटल और एनालॉग वीएलएसआई डिजाइन, एफपीजीए कार्यान्वयन और डिजाइन स्वचालन जैसे उन्नत विषयों के साथ-साथ कैडेंस और जिलिनक्स विवाडो जैसे उद्योग-मानक उपकरणों का उपयोग करके व्यावहारिक सत्रों को शामिल करके अकादमिक शिक्षण और उद्योग की मांगों के बीच की खाई को पाटना था। इस कार्यक्रम में 13 राज्यों के 28 संस्थानों के 50 प्रतिभागियों ने भाग लिया, जिनमें प्रसिद्ध संस्थानों के संकाय, शोध विद्वान और जेआरएफ शामिल थे। सी-डैक मोहाली के निदेशक वीके शर्मा एफडीपी के मुख्यअतिथि थे। उन्होंने वीएलएसआई शिक्षा और उद्योग सहयोग को आगे बढ़ाने में कार्यक्रम के महत्व पर प्रकाश डाला। दिल्ली विश्वविद्यालय से डॉ. मनोज सक्सेना और सीडैक मोहाली से डॉ. बलविंदर सिंह क्रमशः विशिष्ट अतिथि और सम्मानीय अतिथि थे। आईआईटी दिल्ली से प्रो. राजेंद्र सिंह, आईआईटी रुड़की से प्रो. सुदेब दास गुप्ता, एचएस जट्टाना जो पहले ऐससीएल मोहाली और इसरो में समूह प्रमुख के रूप में कार्य कर चुके हैं और सीडैक मोहाली के विशेषज्ञ एफडीपी में व्यावहारिक परियोजनाओं के साथ-साथ व्याख्यान देंगे। एफडीपी का समन्वयन प्रोफेसर श्रुति जैन, डॉ. विकास बघेल, डॉ. निशांत जैन और डॉ. प्रदीप गर्ग ने किया।

एफडीपी में वीएलएसआई शिक्षा और उद्योग में सहयोग पर चर्चा

- एक सप्ताह तक चलेगा कार्यक्रम, विशेषज्ञ देंगे जानकारी

नई दिल्ली, लोकसत्य

जेपी सूचना प्रौद्योगिकी विश्वविद्यालय, सोलन ने इलेक्ट्रॉनिक्स और संचार इंजीनियरिंग विभाग द्वारा सीडैक मोहाली, आई.ई.ई.ई. इंडिया काउंसिल और आई.ई.ई.ई. दिल्ली सेक्शन के सहयोग से आयोजित वीएलएसआई डिजाइनः ब्रिजिंग थ्योरी एंड प्रैक्टिस कार्यक्रम के उद्घाटन की मेजबानी की। यह कार्यक्रम एक सप्ताह तक चलेगा।

एफडीपी (फैकल्टी डेवलपमेंट प्रोग्राम) का उद्देश्य डिजिटल और एनालॉग वीएलएसआई डिजाइन, एफपीजीए कार्यान्वयन और डिजाइन स्वचालन जैसे उन्नत विषयों के साथ-साथ कैडेंस और जिलिनक्स विवाडो जैसे उद्योग-मानक उपकरणों का उपयोग करके व्यावहारिक सत्रों को शामिल करके अकादमिक शिक्षण और उद्योग की मांगों के बीच की खाई को पाटना था। इस कार्यक्रम में 13 राज्यों के 28 संस्थानों के 50 प्रतिभागियों ने भाग लिया। जिनमें प्रसिद्ध संस्थानों के संकाय, शोध विद्वान और जेआरएफ शामिल थे। सी-डैक मोहाली के निदेशक वीके शर्मा एफडीपी के मुख्य अतिथि थे।

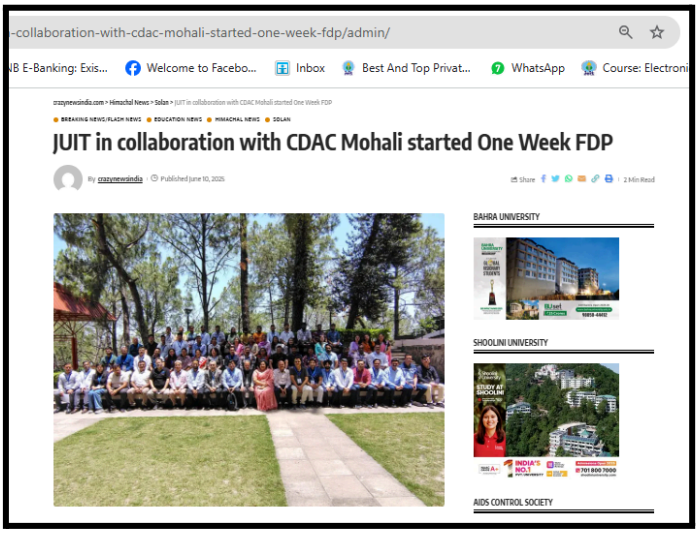
उन्होंने वीएलएसआई शिक्षा और उद्योग में सहयोग को आगे बढ़ाने में कार्यक्रम के महत्व पर प्रकाश डाला। दिल्ली विश्वविद्यालय से डॉ. मनोज सक्सेना विशिष्ट अतिथि और सीडैक मोहाली से डॉ. बलविंदर सिंह सम्मानीय अतिथि थे। आईआईटी दिल्ली से प्रो. राजेंद्र सिंह, आईआईटी रुड़की से प्रो. सुदेब दास गुप्ता, इसरो में समूह प्रमुख रह चुके एच.एस. जट्टाना और सीडैक मोहाली के विशेषज्ञ एफडीपी में व्यावहारिक परियोजनाओं के साथ-साथ व्याख्यान देंगे। एफडीपी का समन्वयन प्रोफेसर श्रुति जैन, डॉ. विकास बघेल, डॉ. निशांत जैन और डॉ. प्रदीप गर्ग ने किया।

Chandigarh 12-06-2025
http://epaper.loksatya.com/

लोकसत्य

"वी.एल.एस.आई. डिजाइन: ब्रिजिंग थ्योरी एंड प्रैक्टिस" नामक प्रभावशाली एक सप्ताह के संकाय विकास कार्यक्रम के उद्घाटन की मेजबानी https://asarnewz.com/?p=52531

JUIT in collaboration with CDAC Mohali started One Week FDP ☞ https://crazynewsindia.com/juit-in-collaboration-with-cdac-mohali-started-one-week-fdp/admin/



Department of Electronics & Communication Engineering, Jaypee University of Information Technology, Solan in collaboration with CDAC Mohali Started One Week FDP on “VLSI Design: Bridging Theory and Practice” https://shikharnewsindia.com/archives/3490