

## VLSI Circuits and System Design (Core Subject)

<b>Course Code:</b>	10M11EC114	<b>Semester:</b>	M.Tech 1 <sup>st</sup> Sem
<b>Credits:</b>	3	<b>Contact Hours:</b>	L-3, T-0,P-0

### Course Objectives

The objectives are to study

1. To bring both Circuits and System views on design together.
2. It offers a profound understanding of the design of complex digital VLSI circuits, computer aided simulation and synthesis tool for hardware design.

### Course Outcomes

After studying this course the students would gain enough knowledge

1. To learn concept of design rules.
2. To bring both Circuits and System views on design together. It offers a profound understanding of the design of complex digital circuits.
3. Synthesis of digital VLSI systems from register-transfer or higher level descriptions in hardware design languages.
4. To be aware about the trends in semiconductor technology, and how it impacts scaling and performance.
5. Understanding a hardware design language such as VHDL in detail – syntax as well as how it works under the hood for simulation and synthesis. To gain enough knowledge to design any circuit using CMOS and write HDL code for any circuit.

### Course Contents

Unit	Topics	References (chapter number, page no. etc)	Lectures
1.	A Brief History and Need of Integrated Circuits, Complexity of VLSI Design: Design Hierarchy, VLSI Design Cycle, Physical Design Cycle, Analog Design Flow, Digital Design Flow, Introduction to MOS Technology and its Electrical Properties, Basic Logic gates : n FET, P FET, CMOS: NOT gate, NAND gate, NOR gate, Stick Diagram, Layout.	John P. Uyemura : Chapter 1, 2	2  4
2.	Basic MOS transistors, Enhancement mode transistor action, Depletion mode transistor action, nMOS fabrication, CMOS fabrication, Drain to source current $I_{ds}$ versus voltage $V_{ds}$ relationships (Non saturated region, Saturated region), MOS transistor transconductance $g_m$ and output conductance $g_{ds}$ , figure of merit, MOS resistance and capacitance, MOS transistor circuit model	Kang : Chapter 3	12
3	nMOS inverter, Determination of pull up and pull down ratio for an nMOS inverter driven by another n MOS inverter, CMOS inverter, DC Characteristics of the CMOS Inverter , Inverter Switching Characteristics, Power Dissipation, DC	Kang : Chapter 4, 5	8

	Characteristics: NAND and NOR Gates, NAND and NOR Transient Response, Analysis of Complex Logic Gates, Gate Design for Transient performance, MOS circuit design process(STICK DIAGRAMS)		
4	Transmission Gates , Gate Delays, Driving Large Capacitive loads, Logical Efforts, Mirror Circuits, Pseudo-nMOS, Tri State Circuits, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-Rail Logic Networks, BiCMOS	Uyemura : Chapter 4, 5	10
5	<b>System Specification Using Verilog HDL :</b> Basic Concepts, Structural Gate-Level Modeling, Switch-level Modeling, Design Hierarchies, Behavioral and RTL Modeling  <b>General VLSI System Components:</b> Gates Adders (Half and Full), Subtractors (Half and Full), Multipliers, Binary Decoders, Equality Detectors and Comparators, Priority Encoder, Shift and rotation Operation, Latches, D Flip-Flop, Registers  <b>System Specification using SPICE :</b> By programming and by circuit level ,Gates (using Diodes, BJT and CMOS)	Uyemura : Chapter 6, 7	8
<b>Total Number of Lectures</b>			44

### Evaluation Scheme

1. Test 1 :15 marks
2. Test 2 : 25 marks
3. Test 3 : 35 marks
4. **Internal Assessment** : 25 marks
  - 10 Marks : Class performance & Assignments
  - 10 Marks : Quizzes
  - 5 marks : Attendance

### Text Books

1. John P. Uyemura: Introduction to VLSI Circuits and Systems, Wiley Student Edition
2. Sung-Mo (Steve) Kang, Yusuf Leblebici, CMOS DIGITAL INTEGRATED CIRCUITS ANALYSIS & DESIGN 3rd Edition, Mc Graw-Hill 2003.J.

### Reference Books

1. Bhasker , “A VHDL Primer”, Pearson Education, 3rd Edition
2. Adel S. Sedra, Kenneth C. Smith : Microelectronics Circuits, 5th Ed., Oxford University Press, 2004
3. Jan M. Rabaey et al , Digital Integrated Circuits : A design Perspective, 2<sup>nd</sup> Edition

### Web Resources

1. URL1:- <http://nptel.ac.in/courses/117106093/>
2. URL2:- <http://nptel.ac.in/courses/Webcourse-contents/IIT-Bombay/VLSI%20Design/Course%20Objective.html>