15B28CI781: High Performance Computing Lab

Course Credit: 1
Semester: VII

Introduction

It is a course which covers the design of advanced modern computing systems. In particular, the design of modern microprocessors, characteristics of the memory hierarchy, and issues involved in multi-threading and multi-processing are discussed. The main objective of this course is to provide students with an understanding and appreciation of the fundamental issues and tradeoffs involved in the design and evaluation of modern computers. Topics will include cost/performance analysis, design and evaluation of instruction set architectures, pipelining techniques, multi-level memory hierarchies, superscalar processor design, multi-threading and multi-processing. Through programming and analysis assignments students will build, in stages, a timing simulator for a simplified out-of-order multiple-issue microprocessor in order to examine the impact of various architectural techniques.

Course Objectives (Post-conditions)

Knowledge objectives:

At the conclusion of the course, following learning objectives are expected to be achieved:

1. You will gain basic knowledge required to design an anlyze high performance computer systems.
2. You will learn how to evaluate and analyze cost and performance of multi processor systems.
3. You will learn various type of interconnection networks used to achive high performance in modern systems
4. You will acquire the background for understanding next-generation GPUs using CUDA.

Application objectives:

The project and homework portions of the course are intended to help you apply your understanding,

1. To develop and simulate assembly language programs on pipelined and serial architecture.
2. To develop, implement, and demonstrate the learning through a project that meet stated specifications.
3. To develop, implement and debug CUDA language program that meet stated specifications.
4. To understand and be able to explain different parallel architectures, interconnections and various memory organization in modern high performance architectures.

Expected Student Background (Preconditions)

Students are expected to have a solid grasp of the fundamentals of computer system, c programming, including a basic understanding of computer organization and microcontrollers. In

addition, students are expected to know application development environment and programming concepts

Topics Outline:

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1	Introduction To Message Passing Interface
2	Communication Between MPI Process: Blocking Operation
3	Communication Between MPI Process: Non-Blocking Operation
4	Collective Communication In MPI: Broadcast and Reduce
5	Collective Communication In MPI: Scatter and Gather
6	Parallel Processing on Shared Memory
7	Introduction To OpenMp
8	Study Parallel Loops
9	Introduction To CUDA programming
10	Study of performance improvement of GPU over parallel program

References

1. Advanced Computer Architecture, Parallelism, Scalability, Programmability, Kai Hwang, Mc Graw Hill International Editions, Computer Science Series.
2. Parallel Programming in C with MPI and OpenMP by M J Quinn
3. Parallel Programming in OpenMP , by Rohit Chandra (Author), Leo Dagum (Author), Dror Maydan

Evaluation Scheme:

1.	Mid Term Exam (Viva and Written Exam)	20
2.	End term Exam (Viva and Written Exam)	30
3.	Lab Records	5
4.	Regular Assessment (Quality and quantity of experiment performed, Learning laboratory skills, Attendance etc.)	30
5.	Project	15
	Total	**100**